What is claimed is:

Claims:

1. A vertical semiconductor device structure, comprising:

a substrate defining a substantially horizontal plane;

a gate electrode projecting vertically from said substrate and including a vertical sidewall;

a spacer flanking said vertical sidewall;

a semiconducting nanotube positioned between said gate electrode and said spacer and extending between opposite first and second ends with a substantially vertical orientation;

a gate dielectric disposed on said vertical sidewall between said nanotube and said gate electrode;

a source electrically coupled with said first end of said nanotube; and

a drain electrically coupled with said second end of said nanotube.

2. The semiconductor device structure of claim 1 wherein said source comprises a catalyst material effective for synthesizing said semiconducting nanotube by a chemical vapor deposition process.

3. The semiconductor device structure of claim 1 wherein said drain comprises a catalyst material effective for synthesizing said semiconducting nanotube by a chemical vapor deposition process.

4. The semiconductor device structure of claim 1 wherein said spacer is separated from said substrate by a gap, said gap being filled by an insulating material after said semiconducting nanotube is formed.

5. The semiconducting device structure of claim 1 wherein said semiconducting nanotube is composed of arranged carbon atoms.

6. The semiconducting device structure of claim 1 wherein said spacer is separated from said vertical sidewall by a passage.

7. The semiconducting device structure of claim 6 wherein said passage has horizontal dimensions appropriate for the growth of said semiconducting nanotube and a vertical dimension greater than or equal to a vertical height of said vertical sidewall of said gate electrode.

8. The semiconducting device structure of claim 6 wherein said passage has a rectangular cross-sectional profile when viewed in a vertical direction.

9. The semiconducting device structure of claim 6 wherein said source is composed of a catalyst material effective for synthesizing said semiconducting nanotube by a chemical vapor deposition process, said source positioned on said substrate in vertical alignment with said passage.

10. The semiconducting device structure of claim 9 wherein said spacer is vertically spaced relative to said substrate to define a gap effective for providing a reactant to said catalyst material of said source effective to grow said semiconducting nanotube by a chemical vapor deposition process.

11. The semiconducting device structure of claim 10 wherein said gap is filled by an insulating material after said semiconducting nanotube is grown by a chemical vapor deposition process.

12. The semiconducting device structure of claim 6 further comprising a plurality of semiconducting nanotubes positioned horizontally between said gate electrode and said spacer, each of said plurality of semiconducting nanotubes extending vertically in said passage between opposite first and second ends.

13. The semiconducting device structure of claim 12 wherein space within said passage not occupied by said plurality of semiconducting nanotubes is filled by an insulating material.

14. The semiconducting device structure of claim 1 further comprising a plurality of semiconducting nanotubes positioned horizontally between said gate electrode and said spacer, each of said plurality of semiconducting nanotubes extending vertically between opposite first and second ends.

15. The semiconducting device structure of claim 14 wherein at least one of said plurality of semiconducting nanotubes has said first end electrically coupled with said source and said second end electrically coupled with said drain.

16. A method of forming a semiconductor device structure, comprising:

forming a catalyst pad on a substrate;

forming a gate electrode adjacent to the catalyst pad;

forming a first spacer on a vertical sidewall of the gate electrode at a position overlying the catalyst pad;

forming a second spacer on the first spacer;

removing the first spacer to define a passage bounded between the second spacer and the gate electrode in which the passage has an open mouth at one end and the catalyst pad situated at the opposite end;

forming a gate dielectric on the vertical sidewall; and

synthesizing a semiconducting nanotube on the catalyst pad that extends substantially vertically from the catalyst pad to a free end proximate the open mouth of the passage.

17. The method of claim 16 wherein removing the first spacer comprises:

selectively etching the first spacer relative to the gate electrode, the second spacer, and the substrate.

18. The method of claim 17 wherein selectively etching the first spacer further comprises:

isotropically etching the first spacer.

19. The method of claim 16 wherein forming the second spacer further comprises:

anisotropically etching the second spacer.

20. The method of claim 16 wherein forming the gate dielectric further comprises:

oxidizing the sidewall of the gate electrode to form the gate dielectric.

21. The method of claim 16 wherein the first spacer is separated vertically from the substrate by a gap providing a flow path to the catalyst pad, and synthesizing the semiconducting nanotube comprises:

directing a reactant through the flow path defined by the gap capable of chemically reacting at the catalyst pad for synthesizing the semiconducting nanotube.

22. The method of claim 21 wherein the reactant is a carbonaceous reactant and the semiconducting nanotube is a carbon nanotube.

23. The method of claim 21 further comprising:

filling the gap with an insulating material after synthesizing the semiconducting nanotube.

24. The method of claim 16 further comprising:

covering the open mouth of the passage and the gate electrode with a layer of insulating material; and

forming a contact in the layer of insulating material electrically coupled with the free end of the semiconducting nanotube.

25. The method of claim 16 wherein synthesizing the semiconducting nanotube further comprises:

exposing the catalyst pad to a reactant under conditions effective to grow the semiconducting nanotube.

26. The method of claim 25 wherein the first spacer is separated from the substrate by a gap providing a flow path to the catalyst pad, and synthesizing the semiconducting nanotube comprises:

directing the reactant through the gap to chemically react at the catalyst pad for synthesizing the semiconducting nanotube.

27. The method of claim 21 wherein the reactant is a carbonaceous reactant and the semiconducting nanotube is a carbon nanotube.

28. The method of claim 16 further comprising:

forming a third spacer overlapping a covered portion of the catalyst pad and exposing an uncovered portion of the catalyst pad after forming the gate electrode and the catalyst pad; and

removing the uncovered portion of the catalyst pad for reducing a surface area of the catalyst pad.

29. The method of claim 28 wherein removing the exposed portion of the catalyst pad comprises:

selectively etching the uncovered portion of the catalyst pad relative to the gate electrode and the substrate.

30. The method of claim 16 further comprising:

forming a contact electrically coupled with the free end of the semiconducting nanotube.

31. The method of claim 30 wherein the free end of the semiconducting nanotube projects into a metal plug constituting the contact.

32. The method of claim 16 wherein the semiconducting nanotube is a carbon nanotube composed of arranged carbon atoms.

33. The method of claim 16 wherein the gate dielectric is formed without adversely affecting the ability of the catalyst pad to catalyze growth of the semiconducting nanotube.

34. The method of claim 16 wherein the semiconducting nanotube defines a channel region of a field effect transistor having a channel along which current flow is regulated by application of a control voltage to the gate electrode.

35. The method of claim 16 further comprising:

synthesizing a plurality of semiconducting nanotubes positioned between the gate electrode and the spacer, each of said plurality of semiconducting nanotubes extending from the catalyst pad to a free end proximate the open mouth of the passage.

36. The method of claim 35 further comprising:

covering the open mouth of the passage and the gate electrode with a layer of insulating material; and

forming a contact in the layer of insulating material electrically coupled with the free end of at least one of the plurality of semiconducting nanotubes.

37. The method of claim 36 wherein the plurality of semiconducting nanotubes are carbon nanotubes.

38. The method of claim 16 wherein the passage has horizontal dimensions appropriate for the growth of the semiconducting nanotube and a vertical dimension greater than or equal to a vertical height of the vertical sidewall of the gate electrode.

39. The method of claim 38 wherein the passage has a rectangular cross-sectional profile when viewed in a vertical direction.

40. The method of claim 38 wherein the catalyst pad is positioned on the substrate in vertical alignment with the passage.

41. The method of claim 40 wherein the spacer is vertically spaced relative to the substrate to define a gap effective for providing a reactant to the catalyst pad effective to grow the semiconducting nanotube by a chemical vapor deposition process.